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TITLE

DAMASCENE GATE PROCESS

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a damascene gate process, and more particularly to a process of forming damascene gates with a line width of 0.11μm.

Description of the Related Art

As semiconductor manufacturing techniques have advanced, MOS gate length has scaled down to 100nm, and the gate oxide layer is less than 3nm thick. The conventional method of fabricating a gate is described in following. Shallow trench isolations (STI) are formed by SiO_2 in the silicon substrate to define an active area. A gate oxide layer and a poly layer are sequentially formed and planarized. A mask layer is formed to cover the poly layer. The poly layer is defined as a poly gate by photolithography and etching. The substrate is implanted to form a lightly doped drain (LDD), and spacers are then formed.

Deposition, photolithography, and etching are performed repeatedly in the conventional process, thus fabrication costs cannot be reduced. When the polysilicon layer and the oxide layer with the exception of the active area are removed, the oxide layer is easily over-etched, damaging the silicon substrate under the oxide layer, thus other layers formed thereon are not uniform. If the polysilicon layer and the oxide layer with the exception of the active area are not completely

removed, stringers remain between gates or the gate and the bit line, thus short circuits occur in the gates.

SUMMARY OF THE INVENTION

The present invention is directed to a damascene gate process, after defining an active area by shallow trench isolation structures, an opening of a predetermined size is formed, the size of the opening is then reduced by forming a protective spacer, and the opening is filled to complete the damascene gate process.

Accordingly, the present invention provides a damascene gate process. A semiconductor substrate having a pad layer and a etch stop layer formed thereon is provided. An insulating layer is formed to cover the etch stop layer. An opening is then formed by partially removing the insulating layer, the etch stop layer, and the pad layer. A protective spacer is formed on the sidewall of the opening, wherein the top of the protective spacer is lower than the insulating layer. A gate conducting layer is formed in the opening. The protective spacer and the insulating layer are removed to expose a portion of the semiconductor substrate and the etch stop layer. The exposed semiconductor substrate is implanted forming lightly doped drains thereon. A gate spacer is formed to cover the gate conducting layer. The etch stop layer and the pad layer are removed to expose portions of the semiconductor substrate. The exposed semiconductor substrate is implanted, forming a source/drain thereon.

The present invention provides an additional damascene gate process. A semiconductor substrate having a plurality of shallow trench isolation (STI) structures is provided, and

an STI protective layer is formed on each of the STI structures. A pad layer and an etch stop layer are sequentially formed between the STI structures. An insulating layer is formed to cover the STI structures and the etch stop layer. An opening is formed between the structures be partially removing the insulating layer, the etch stop layer, and the pad layer. A protective spacer is formed on the sidewall of the opening, wherein the tops of the protective spacers are lower than the insulating layer. Dissimilar conducting layers are formed, acting as a gate conducting layer, in the bottom of the opening. The protective spacer and the insulating layer are removed to expose a portion of the semiconductor substrate and the etch stop layer. The exposed semiconductor substrate is implanted to form lightly doped drains beside the gate conducting layer. A gate spacer is formed to cover the gate conducting layer. The etch stop layer and the pad layer are removed. The exposed semiconductor substrate is implanted forming a source/drain therein.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference is made to a detailed description to be read in conjunction with the accompanying drawings, in which:

FIGs. 1A to 1O are cross-sections of the damascene gate process of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGs. 1A to 1O are cross-sections of the damascene gate process of the present invention.

In FIG. 1A, a semiconductor substrate 100 having a pad layer 110, such as an oxide layer, is provided, in which two shallow trench isolations (STI) 112, such as oxide layers, are formed in predetermined regions to define an active area. An STI protective layer 114 of dielectric material, such as nitride, is formed on each STI 112. In this invention, the STI protective layer 114 can be formed by LPCVD using $SiCl_2H_2$ and NH_3 as reaction sources at a temperature of 250 to 400°C.

In FIG. 1B, a etch stop layer 115, such as silicon nitride, is formed on pad oxide layer 110 in the active area, and an insulating layer 116, such as tetraethylorthosilane (TEOS), is formed by chemical vapor deposition (CVD) or thermal oxidation. A patterned photoresist layer having an opening is formed on the insulating layer 116. The insulating layer 116 and the pad oxide layer 110 are sequentially etched until the semiconductor substrate is exposed to form an opening 118.

In FIG. 1C, a sacrificial layer 120 is formed to cover the insulating layer 116 and fill in the opening 118. In this invention, the sacrificial layer 120 can be formed by LPCVD using $SiCl_2H_2$ and NH_3 as reaction sources at a temperature of 250 to 400°C. The sacrificial layer 120 is subject to chemical mechanical polishing (CMP) or etching to remove the portion of the sacrificial layer 120 covering the insulating layer 120, thus, sacrificial layer 120' is lower than the insulating layer 116 as shown in FIG. 1D.

In FIG. 1E, a material of high etch selectivity with respect to the sacrificial layer, such as a poly layer 122, is conformably formed to cover the insulating layer 116 and the sacrificial layer 120'. In this invention, the sacrificial layer 120 can be formed by LPCVD using a mixture of materials

containing silicon, such as $SiCH_4$, as reaction sources at a temperature of 530 to 650°C.

In FIG. 1F, a patterned photoresist layer defining a gate area is formed. The poly layer and the sacrificial layer are etched to form an opening 119. After etching the poly layer 122' and the protective spacer 120'' remain, and the size of the opening is reduced to 0.09μm.

In FIG. 1G, the remained poly layer 122' is wet etched by NH_4OH.

In FIG. 1H, a gate dielectric layer, such as a thin SiO_2 layer, is formed on the exposed semiconductor substrate by thermal oxidation. A first conducting layer 124, such as a poly layer, is fully formed to cover the insulating layer 116 and fill in the opening 119.

In FIG. 1I, the first conducting layer 124 is subject to CMP or etching to form an N+ type poly layer 124'. In this invention, the thickness of the first conducting layer 124' is 2500 to 5000Å, and can be formed by LPCVD at a temperature of 530 to 650°C. For an N+ type element, the poly layer can be doped in situ in a gas mixture containing SiH_4, phosphine or arsine. The doped poly layer also can be formed by implanting phosphorous or arsenic ions into the poly layer.

In FIG. 1J, a conducting layer 126, such as W, silicide, or WSi_x layer, acting as a gate conducting layer is formed to cover the insulating layer 116 and fill in the opening 119. In this invention, the thickness of the conducting layer 126 is 1500 to 4500Å, and can be formed by LPCVD using SiH_4 or $SiCl_2H_2$ (DCS) and WF_6 as reaction sources at a temperature of 300 to 600°C under pressure of 100 to 500mTorr.

In FIG. 1K, the conducting layer 126 is subject to CMP or etching to form a conducting layer 126', and the height of the conducting layer 126' is either equal or unequal to the protective spacer 120''.

In FIG. 1L, the protective layer 120'' is removed by dry etching, and a laminated construction acting as a damascene gate conducting layer consists of the first conducting layer and the second conducting layer.

In FIG. 1M, the insulating layer 116 is removed by HF or BHF.

In FIG. 1N, the exposed semiconductor substrate is implanted with 10 keV acceleration energy and a 1×10^{13} to 3×10^{13} cm^{-2} dose to form lightly doped drains (LDD) 128 beside the laminated construction.

In FIG. 1O, a dielectric layer acting as a gate spacer 130, such as a silicon nitride layer, is formed, the pad layer 115' and 110' are removed, and source/drain 132 are formed in the semiconductor substrate by implantation, thus a damascene gate process is complete.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.